UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/737,418	12/15/2003	Steven E. Molnar	NVDA/P001024	6363

26291 7590 03/22/2005

MOSER, PATTERSON & SHERIDAN L.L.P.
595 SHREWSBURY AVE, STE 100
FIRST FLOOR
SHREWSBURY, NJ 07702

EXAMINER	
CASCHERA, ANTONIO A	
ART UNIT	PAPER NUMBER
2676	

DATE MAILED: 03/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/737,418	MOLNAR ET AL.	
	Examiner	Art Unit	
	Antonio A Caschera	2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 December 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

The abstract comprises the sentence, "Apparatuses and methods for detecting position conflicts during fragment processing are described," (see lines 1-2 of abstract) which can be implied and therefore should be omitted.

Drawings

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: #827 of Figure 8C and #1127 of Figure 11B. Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are

not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

3. Claims 6 and 18 are objected to because of the following informalities:

a. In reference to claim 6, the phrase, "less that," (see line 2 of claim 6) should be corrected to, "less than."

b. In reference to claim 18, claim 18 incorrectly claims dependency upon itself. A correction is required as to the dependency of claim 18. For the following prior art rejections, the office will assume claim 18 is dependent upon claim 11.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by Wood et al. (U.S. Patent 6,204,856 B1).

In reference to claim 1, Wood et al. discloses a method and apparatus for handling texture and other attributes in rendering of graphic images (see column 1, lines 4-6). Wood et al. discloses partitioning an image into tiles, each tile associated with a unique tile origin defined by a, "magic point" which is associated with a pixel center (see column 4, lines 41-43 and 56-60). Wood et al. also discloses allocating an entry in a buffer memory for holding tile data defined as tile fragment stacks, which hold face identifier data which the office interprets functionally equivalent to the "tile number" of applicant's claim (see column 5, lines 1-14). Note, the office interprets Wood et al. to inherently store a potion of a position associated with a fragment in the tile fragment stack as triangles are tested to see if they overlap a tile and recorded as an entry in the tile fragment stack (see column 4, lines 44-52 and column 5, lines 1-14).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 2, 5, 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wood et al. (U.S. Patent 6,204,856 B1) in view of Kent (U.S. Publication 2003/0164830 A1).

In reference to claim 2, Wood et al. discloses all of the claim limitations as applied to claim 1 above however, Wood et al. does not explicitly disclose storing a coverage mask associated with a fragment in memory. Kent discloses new innovations to 3D graphics computer systems, including a 3D graphics chip implementing texturing, filtering and lighting techniques

(see paragraphs 1, 19-20 and Figure 1A). Kent discloses the graphics accelerator chip to include a rasterizer which operates upon 2D and 3D primitives, broken up into tiles for processing (see lines 1-3 of paragraph 49). Kent also discloses that each tile comprises an 8x8 square of pixels and is screen aligned (see lines 3-4 of paragraph 49). Kent further discloses a memory unit organized to store these tiles linearly (see paragraph 124, last 3 lines). Kent discloses computing a tile mask to show which fragments in each tile are inside a primitive and storing the tile mask within memory (see paragraph 131 and last 4 lines of paragraph 177). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the tile fragmenting techniques of Wood et al. with the tile masking techniques of Kent in order to provide an improved accuracy of tiling in a tile-based rendering system, saving memory bandwidth (see column 1, lines 45-50 and column 2, lines 36-39 of Wood et al.).

In reference to claim 5, Wood et al. and Kent disclose all of the claim limitations as applied to claim 2 above in addition, Kent discloses ANDing together different masks representing edges of primitive fragments to return a tile mask with the inside fragments of a primitive for a specific tile set (paragraph 133). Kent also discloses storing the tile mask within memory (see last 4 lines of paragraph 177).

In reference to claim 6, Wood et al. and Kent disclose all of the claim limitations as applied to claim 1 above, neither Wood et al. nor Kent explicitly disclose the number of entries in memory being less than the number of tiles in the image however, at the time the invention was made, it would have been obvious to one of ordinary skill in the art to implement a memory architecture in Wood et al. or Kent that is capable of storing less data than represented upon a display device. Applicant has not disclosed that having memory resources to store less data than

represented by an image on a screen provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with the storing of each tile of an image in tile fragment stack buffer of Wood et al. because such a system configuration is a matter of design choice as preferred by the designer and to which best suits the application at hand. Therefore, it would have been obvious to one of ordinary skill in this art to modify Wood et al. and Kent to obtain the invention as specified in claim 6.

6. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wood et al. (U.S. Patent 6,204,856 B1) in view of Robotham et al. (U.S. Patent 6,704,024 B2).

In reference to claim 4, Wood et al. discloses all of the claim limitations as applied to claim 1 above however, Wood et al. does not explicitly disclose storing a timestamp value in a memory entry. Robotham et al. discloses a server/client system for browsing visual content using rasterized representations (see column 1, lines 13-20) wherein the client can store a timestamp value with a cached representation of the content for determinations of whether refresh actions are required (see column 45, lines 52-63). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the timestamp refreshing techniques of Robotham et al. with the tile fragmenting techniques of Wood et al. in order to update memory caches which satisfy user preferred viewing visual content in graphics systems (see column 45, lines 29-35 of Robotham et al.).

7. Claims 3, 7, 8, 10-15 and 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wood et al. (U.S. Patent 6,204,856 B1), Kent (U.S. Publication 2003/0164830 A1) and further in view of Saito et al. (U.S. Publication 2004/0212619 A1).

In reference to claim 3, Wood et al. and Kent disclose all of the claim limitations as applied to claim 1 above. Neither Wood et al. nor Kent explicitly disclose storing a tile state in memory however Saito et al. does. Saito et al. discloses an image rendering device and method which divides image data into, "chunks" representing 8x8 pixel areas (see paragraph 3 and paragraph 61, lines 1-7). Saito et al. discloses further dividing chunks into, "stamps" which are smaller 2x2 area pixels of chunk data (see paragraph 94, lines 1-4). Saito et al. discloses determining merging chunk data whereby conflicting chunk data is determined via a pixel-by-pixel basis (see paragraph 92, lines 1-4). Within the chunk merging process, Saito et al. discloses storing the status of chunk pixels, storing whether a write has been performed to each of the pixels as a status in a chunk data buffer (see paragraph 70, lines 1-3 and paragraph 72). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the tile fragmenting techniques of Wood et al. and tile masking techniques of Kent with the pixel status storing techniques of Saito et al. in order to save processing cycles and therefore produce a more efficient image rendering system when required to determine which pixels need to be processed by storing a status for each pixel, allowing for only those pixels which require processing to be performed upon (see paragraphs 7-8 of Saito et al.).

In reference to claim 7, Wood et al. and Kent disclose all of the claim limitations as applied to claim 1 above. Neither Wood et al. nor Kent explicitly disclose outputting the position associated with at least one fragment when a conflict does not exist. Saito et al. discloses an image rendering device and method which divides image data into, "chunks" representing 8x8 pixel areas (see paragraph 3 and paragraph 61, lines 1-7). Saito et al. discloses further dividing chunks into, "stamps" which are smaller 2x2 area pixels of chunk data (see

paragraph 94, lines 1-4). Saito et al. discloses determining merging chunk data whereby conflicting chunk data is determined via a pixel-by-pixel basis (see paragraph 92, lines 1-4). Saito et al. discloses that when no conflict is detected, pixel data is written into the existing chunk (see paragraph 89, last 3 lines) which the office interprets as outputting the position associated with at least one fragment since pixels comprise of position data and such data is represented by a fragment as non-conflicted data (see Figure 14). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the tile fragmenting techniques of Wood et al. and tile masking techniques of Kent with the pixel status storing techniques of Saito et al. in order to save processing cycles and therefore produce a more efficient image rendering system when required to determine which pixels need to be processed allowing data which does not conflict with other data to be properly displayed and therefore allowing for only those pixels which require processing to be performed upon (see paragraphs 7-8 of Saito et al.).

In reference to claim 8, Wood et al. and Kent disclose all of the claim limitations as applied to claim 1 above. Neither Wood et al. nor Kent explicitly disclose outputting a token when a predetermined number of quads are received. Saito et al. discloses an image rendering device and method which divides image data into, "chunks" representing 8x8 pixel areas (see paragraph 3 and paragraph 61, lines 1-7). Saito et al. discloses further dividing chunks into, "stamps" which are smaller 2x2 area pixels of chunk data (see paragraph 94, lines 1-4). Saito et al. discloses determining merging chunk data whereby conflicting chunk data is determined via a pixel-by-pixel basis (see paragraph 92, lines 1-4). Saito et al. also discloses outputting an overflow signal to a signal generator which determines whether to generate a chunk flush signal

(see paragraph 73 and Figure 8). Note, the office interprets that since the overflow signal triggers a flush of memory, the overflow signal is seen as functionally equivalent to the token of applicant's claim while the number of quads of applicant's claim refers to the number of chunks in Saito et al., which are already stored and waiting to be flushed out. It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the tile fragmenting techniques of Wood et al. and tile masking techniques of Kent with the pixel status storing techniques of Saito et al. in order to save processing cycles and therefore produce a more efficient image rendering system when required to determine which pixels need to be processed allowing data which does not conflict with other data to be properly displayed and therefore allowing for only those pixels which require processing to be performed upon (see paragraphs 7-8 of Saito et al.).

In reference to claim 10, Wood et al. and Kent disclose all of the claim limitations as applied to claim 1 above. Neither Wood et al. nor Kent explicitly disclose outputting a token when a conflict is detected. Saito et al. discloses an image rendering device and method which divides image data into, "chunks" representing 8x8 pixel areas (see paragraph 3 and paragraph 61, lines 1-7). Saito et al. discloses further dividing chunks into, "stamps" which are smaller 2x2 area pixels of chunk data (see paragraph 94, lines 1-4). Saito et al. discloses determining merging chunk data whereby conflicting chunk data is determined via a pixel-by-pixel basis (see paragraph 92, lines 1-4). Saito et al. also discloses setting various flags when a conflict is detected including a valid and compare flag (see paragraphs 111, 113 and 114), which the office interpret as functionally equivalent to the token of applicant's claim. It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the tile

fragmenting techniques of Wood et al. and tile masking techniques of Kent with the pixel status storing techniques of Saito et al. in order to save processing cycles and therefore produce a more efficient image rendering system when required to determine which pixels need to be processed allowing data which does not conflict with other data to be properly displayed and therefore allowing for only those pixels which require processing to be performed upon (see paragraphs 7-8 of Saito et al.).

In reference to claim 11, Wood et al. discloses a method and apparatus for handling texture and other attributes in rendering of graphic images (see column 1, lines 4-6). Wood et al. discloses partitioning an image into tiles, each tile associated with a unique tile origin defined by a, "magic point" which is associated with a pixel center (see column 4, lines 41-43 and 56-60). Wood et al. also discloses allocating an entry in a buffer memory for holding tile data defined as tile fragment stacks, which hold face identifier data which the office interprets functionally equivalent to the "tile number" of applicant's claim (see column 5, lines 1-14). Note, the office interprets Wood et al. to inherently store a potion of a position associated with a fragment in the tile fragment stack as triangles are tested to see if they overlap a tile and recorded as an entry in the tile fragment stack (see column 4, lines 44-52 and column 5, lines 1-14). Wood et al. does not explicitly disclose storing a coverage mask associated with a fragment in memory. Kent discloses new innovations to 3D graphics computer systems, including a 3D graphics chip implementing texturing, filtering and lighting techniques (see paragraphs 1, 19-20 and Figure 1A). Kent discloses the graphics accelerator chip to include a rasterizer which operates upon 2D and 3D primitives, broken up into tiles for processing (see lines 1-3 of paragraph 49). Kent also discloses that each tile comprises an 8x8 square of pixels and is screen aligned (see lines 3-4 of

paragraph 49). Kent further discloses a memory unit organized to store these tiles linearly (see paragraph 124, last 3 lines). Kent discloses computing a tile mask to show which fragments in each tile are inside a primitive and storing the tile mask within memory (see paragraph 131 and last 4 lines of paragraph 177). Saito et al. discloses an image rendering device and method which divides image data into, "chunks" representing 8x8 pixel areas (see paragraph 3 and paragraph 61, lines 1-7). Saito et al. discloses further dividing chunks into, "stamps" which are smaller 2x2 area pixels of chunk data (see paragraph 94, lines 1-4). Saito et al. discloses determining merging chunk data whereby conflicting chunk data is determined via a pixel-by-pixel basis (see paragraph 92, lines 1-4), such determinations performed by a chunk flush controller (see paragraph 80) which the office interprets functionally equivalent to applicant's control unit. Within the chunk merging process, Saito et al. discloses storing the status of chunk pixels, storing whether a write has been performed to each of the pixels as a status in a chunk data buffer (see paragraph 70, lines 1-3 and paragraph 72). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the tile fragmenting techniques of Wood et al. and tile masking techniques of Kent with the pixel status storing techniques of Saito et al. in order to save processing cycles and therefore produce a more efficient image rendering system when required to determine which pixels need to be processed by storing a status for each pixel, allowing for only those pixels which require processing to be performed upon (see paragraphs 7-8 of Saito et al.).

In reference to claims 12 and 14, Wood et al., Kent and Saito et al. disclose all of the claim limitations as applied to claim 11 above. Claims 12 and 14 are equivalent in scope to claims 10 and 8 respectively and therefore are rejected under similar rationale in addition

however, Saito et al. does not explicitly disclose the chunk flush controller specifically outputting flag data or overflow signal. At the time the invention was made, it would have been obvious to one of ordinary skill in the art to allow the conflict determination element to output a token signal when data conflicts are detected or a predetermined number of data received. Applicant has not disclosed that having the control unit explicitly output a token and not another element provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with the flag data and signal setting techniques of Saito et al. because setting the exact element which signals when a conflict is detected or when a predetermined number of data is received is seen as a matter of design choice as preferred by the designer and to which best suits the application at hand. Therefore, it would have been obvious to one of ordinary skill in this art to modify Wood et al., Kent and Saito et al. to obtain the invention as specified in claims 12 and 14.

In reference to claim 13, Wood et al., Kent and Saito et al. disclose all of the claim limitations as applied to claim 1 above. Saito et al. also discloses outputting an overflow signal to a signal generator which determines whether to generate a chunk flush signal (see paragraph 73 and Figure 8). Note, the office interprets that since the overflow signal triggers a flush of memory, the overflow signal is seen as functionally equivalent to the token of applicant's claim. Also note, the overflow signal of Saito et al. is interpreted to signify when memory storage is full or at least close to be being full, hence it triggers a flush of chunk data. At the time the invention was made, it would have been obvious to one of ordinary skill in the art to output a token when memory space is limited. Applicant has not disclosed that having the control unit explicitly

output this token and not another element provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with the flag data and signal setting techniques of Saito et al. because the setting the exact element which signals when a predetermined number of data is received is seen as a matter of design choice as preferred by the designer and to which best suits the application at hand. Therefore, it would have been obvious to one of ordinary skill in this art to modify Wood et al., Kent and Saito et al. to obtain the invention as specified in claim 13.

In reference to claim 15, Wood et al., Kent and Saito et al. disclose all of the claim limitations as applied to claim 11 above. Claim 15 is equivalent in scope to claim 5 and therefore is rejected under similar rationale.

In reference to claims 18 and 20, Wood et al., Kent and Saito et al. disclose all of the claim limitations as applied to claims 11 and 19 respectively. Wood et al. discloses implementing a fragment tile buffer whereby data is read from and a FIFO buffer for storing the rendered tiles (see column 10, lines 41-44 and column 5, lines 23-25). Since Wood et al. discloses reading and writing (rendered tiles are written to FIFO buffer) data to buffer memories, the office interprets that Wood et al. inherently discloses a read and a write interface.

In reference to claim 19, Wood et al., Kent and Saito et al. disclose all of the claim limitations as applied to claim 11 above. Wood et al. also discloses a main attribute processor for interpolating pixel values and receiving sampled values to perform pixel fragments which are further judged on whether to be impacted by a polygon and stored in a pixel fragment buffer, part

of an auxiliary buffer unit (see column 5, lines 26-35, column 6, lines 27-37, column 7, lines 30-41).

8. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wood et al. (U.S. Patent 6,204,856 B1), Kent (U.S. Publication 2003/0164830 A1), Saito et al. (U.S. Publication 2004/0212619 A1) and further in view of Hinton et al. (U.S. Publication 2003/0115267 A1).

In reference to claim 9, Wood et al., Kent and Saito et al. disclose all of the claim limitations as applied to claim 8 above, however neither Wood et al, Kent nor Saito et al. explicitly disclose updating a timestamp when the token is output. Hinton et al. discloses methods for accessing authorization systems whereby a computer system implements a, "refresh enrollment token" indicating that a user's identity cookie must be refreshed and refreshes the cookie timestamp (see paragraph 7 and paragraph 218). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the timestamp refreshing based upon token techniques of Hinton et al. with the tile fragmenting techniques of Wood et al., tile masking techniques of Kent and pixel status storing techniques of Saito et al. in order to ensure that the most persistent, up-to-date data is kept across multiple interconnected devices (see paragraph 231, lines 1-2 of Hinton et al.) so that these devices may accurately operate with one another and the best output is guaranteed.

9. Claims 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wood et al. (U.S. Patent 6,204,856 B1), Kent (U.S. Publication 2003/0164830 A1), Saito et al. (U.S. Publication 2004/0212619 A1) and further in view of Robotham et al. (U.S. Patent 6,704,024 B2).

In reference to claim 16, Wood et al., Kent and Saito et al. disclose all of the claim limitations as applied to claim 11 above, however neither Wood et al., Kent nor Saito et al. explicitly disclose a timestamp unit configured to maintain a timestamp. Robotham et al. discloses a server/client system for browsing visual content using rasterized representations (see column 1, lines 13-20) wherein the client can store a timestamp value with a cached representation of the content for determinations of whether refresh actions are required (see column 45, lines 52-63). Robotham et al. also discloses the timestamp sent to client from a server (see column 45, lines 53-55). Note, the office interprets that the server of Robotham et al. inherently discloses a timestamp unit configured to maintain a timestamp since it is the element which sends and therefore generates, the timestamp to the client. It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the timestamp refreshing techniques of Robotham et al. with the tile fragmenting techniques of Wood et al., tile masking techniques of Kent and pixel status storing techniques of Saito et al. in order to update memory caches which satisfy user preferred viewing visual content in graphics systems (see column 45, lines 29-35 of Robotham et al.).

In reference to claim 17, Wood et al., Kent, Saito et al. and Robotham et al. disclose all of the claim limitations as applied to claim 16 above. Note, since the server of Robotham et al. sends the timestamp to the client who in turn, stores the timestamp in cache with the visual representation, the office interprets that Robotham et al. inherently copies the timestamp from server to client.

References Cited

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

a. Duluk, Jr. et al. (U.S. Patent 6,717,576 B1)

- Duluk, Jr. et al. discloses a deferred shading graphics pipeline processor and method including a tiled frame buffer memory.

b. Zhu et al. (U.S. Patent 6,323,860 B1)

- Zhu et al. discloses a method performed in a graphics processor for identifying changes to a rendering tile state using timestamps.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Antonio Caschera whose telephone number is (703) 305-1391. The examiner can normally be reached Monday-Thursday and alternate Fridays between 7:00 AM and 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Bella, can be reached at (703)-308-6829.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

aac

3/15/05

MATTHEW C. BELLA
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600